ECE 120A Final Lab

Robin Teng, Maxwell Wu, Deven Tseng, and Thomas Duan
Department of Electrical and Computer Engineering, University of California, Santa Barbara

Mark Zakharyan and Chengxuan Li
Department of Physics, University of California, Santa Barbara

(Dated: March 19, 2025)

This report details the fabrication steps and electrical characterization of several electric devices. These include metal oxide semiconductor field effect transistors (MOSFETs), PN diodes, MOSCAPS, resistors, and TLM pads. The fabrication sequence involved oxidation, photolithography, diffusion, etching, and metallization to create fully functional transistors. We characterized the devices using electrical measurements, including I-V and C-V analysis, to extract key performance parameters. The MOSFET displayed a body to gate breakdown voltage of 18V and a transconductance of 1.923mS for the 100μm x 10uμm NMOS. The diodes had a breakdown voltage past -40V–beyond the measurable limit of the hp4145A semiconductor analyzer and a ideality factors of 1.91.

I. INTRODUCTION

The fabrication and characterization of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are essential for understanding modern semiconductor technology. MOSFETs serve as the foundation of integrated circuits, enabling the operation of microprocessors, memory devices, and various analog and digital applications. This experiment provides hands-on experience in the step-by-step fabrication of an n-channel MOSFET, reinforcing theoretical concepts related to semiconductor processing and device physics. Additionally, the lab includes the fabrication and testing of other semiconductor devices, such as p-n junction diodes, MOS capacitors, and silicon resistors, allowing for a broader understanding of integrated device fabrication.

The fabrication process involves the use of four mask layers to define different regions of the MOSFET and other devices. It begins with the oxidation of a p-type silicon wafer to form an insulating silicon dioxide layer. Photolithography and etching are then used to selectively remove oxide and expose regions for doping. Phosphorus diffusion is performed to create the n-type source and drain regions. A thin gate oxide is then grown, followed by the deposition and patterning of metal contacts. Throughout the process, precise alignment of each mask layer is crucial to ensure proper functionality of all fabricated devices.

Once fabrication is complete, a comprehensive electrical characterization is undertaken to evaluate device performance and extract critical figures-of-merit. This phase incorporates a range of measurement techniques—such as current-voltage (I-V) and capacitance-voltage (C-V) analyses using both 2-probe and 4-probe setups—to thoroughly assess each device type. Specifically:

- **Transmission Line Method (TLM) Structures:** I-V measurements on TLM pads, using both 2-probe and 4-probe configurations, are performed to extract contact resistance and specific contact resistivity. With up to 12 TLM structures per chip, the statistical analysis of these multiple data points yields average values and error estimates.

- ***p-n* Junction Diodes:** Both I-V and C-V measurements are used to determine key diode parameters, including threshold voltage, dark (reverse leakage) current, series resistance, ideality factor, and reverse breakdown voltage. Additionally, C-V data in the reverse bias region are employed to estimate the built-in voltage and acceptor concentration.

- **Transistors:** We established a 5-dimensional polynomial with interactive graphs showing the results of sweeping the gate-source voltage (V_{ds}) under various stepped gate-source voltages (V_{gs}) to observe turn-off characteristics. Also, I-V graph is established by sweeping V_{gs} under various stepped V_{ds} to calculate the transconductance. For C-V measurements, we measured MOSCAPs formed under the gate electrode (gate-body), to compare the characteristics for varying sizes of gates, and the gate-source regions, to extract transfer capacitance. We also determined the flat-band voltage and whether there is a difference in measurements between light and dark.

By successfully fabricating and testing multiple semiconductor devices, this lab bridges the gap between theoretical knowledge and practical semiconductor processing. Understanding the role of each fabrication step, along with the use of multiple mask layers, is essential for anyone working in semiconductor design and manufacturing.

II. METHODOLOGY

A. Sample Preparation

Using one cleaved p-type ⟨100⟩ silicon sample, we first measured the thickness of the wafer, sheet resistance, and sheet resistivity using the Veeco Four-Point Probe. The sheet resistance was measured to be 83.8 Ω/□, and the thickness of the sample was 530 µm. From these measurements, we calculated the sheet resistance according to the following equation:

$$\rho = R_{\text{sheet}} \times t \tag{1}$$

where ρ is the sheet resistivity, R_{sheet} is the sheet resistance, and t is the thickness. This gave a sheet resistivity of about $\rho = 4.4414\,\Omega\,\text{cm}$. Carrier concentration and carrier mobility are related according to the equation [1]

$$\mu = \frac{1}{qN\rho} \tag{2}$$

where the ρ is the resistivity, μ is the carrier mobility, N is the dopant concentration, and q is the charge of an electron. Here, the carrier mobility is assumed to be $450\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$, and so the carrier concentration according to the above equation is computed to be approximately $5.892 \times 10^{16}\,\text{cm}^{-3}$.

B. Mask 1

We were given 4 samples with 4681.94 ± 85.85 Å of field oxide grown on top. The oxide thickness was measured using Filmetrics, where error is the standard deviation across all 4 samples. We then followed the standard solvent cleaning process: sonicating in acetone for 2 minutes, IPA for 2 minutes, rinsing in DI water for 2 minutes, and blow drying with an N_2 gun. The samples were then baked at 130 °C for 3 minutes to dry leftover water residue. Next, the samples underwent HMDS vapor deposition for 3 minutes followed by spin coating of AZ P4110 photoresist at a recipe of 4000 rpm and 30 seconds. The samples were then soft baked on a 95 °C hotplate for 1 minute prior to exposure. The mask 1 pattern (Fig. 1 was aligned on the centers of each sample using a Karl Suss MJB3 aligner. To align the masks perfectly, we create a translational offset between the mask and the pattern on the sample, allowing us to understand the rotational difference between the mask and the pattern. We then adjust the rotation of the stage until the mask became aligned with the sample under the smallest magnification objective. We then proceed to a higher magnification and repeat the previous process. We then superpose the mask and the pattern perfectly, without the translational difference, and use the markers located at the four corners of the pattern for the final alignment under the largest magnification objective Fig. 14.

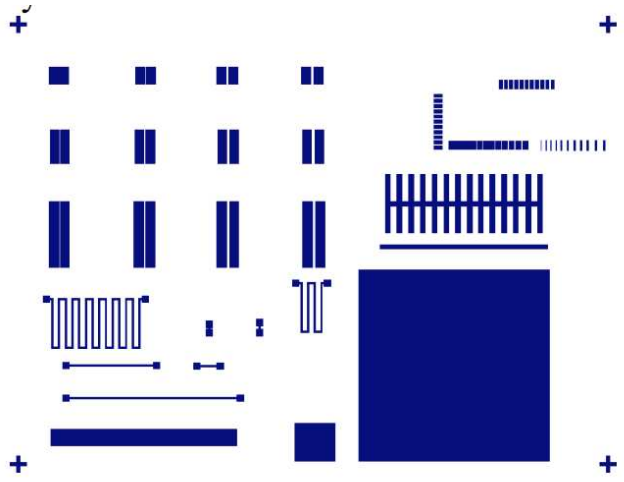

FIG. 1. Mask 1

The required exposure time can be calculated from the equation

$$D = I \times t \tag{3}$$

where D is the dose, I is the irradiance, and t is the exposure time. Given an irradiance of $10\,\text{mW}\,\text{cm}^{-2}$ and a recommended dose of $90\,\text{mJ}\,\text{cm}^{-2}$ as established from previous labs, the samples were exposed for 18 seconds. Next, the samples were developed in 1:4 AZ400K developer solution for 70 s. The result of this process is shown in Fig 2, which shows that exposure and mask alignment successfully generated precise features with high resolution of lithography patterns. After mask 1 photolithography, the samples were hard baked at 120C for 3 minutes to improve resist adhesion, followed by a 1-minute O_2 plasma descum to remove photoresist residue.

The samples were etched in buffered hydrofluoric acid (BHF) to form windows in the field oxide for n-type dopant diffusion. Before etching the samples, we calibrated the etch sample rate by etching a pilot sample in 1 minute increments and subsequently measuring the oxide thicknesses. The etch rate was calculated to be $1095\,\text{Å}\,\text{min}^{-1}$. Thus, the samples were etched for a total of 308 seconds, which includes a 20% overetch to make sure all SiO_2 was etched away in the exposed areas. Profilometer measurements shown in Fig. 3 were taken after this etch as well as after PR removal to confirm that the correct step height profiles were achieved.

The next step in the process is n-type dopant diffusion using phosphorous. Before placing our samples in the diffusion furnace, we solvent cleaned our samples, then performed a 10-minute Piranha clean and 10-second HF dip to clean the surface of the samples and remove the native oxide layer. We then loaded our samples into the diffusion furnace, where the PDS-1000N diffusion sources deposited phosphorous onto the surface of our samples. The diffusion process was performed at a temperature of 950 °C for 20 minutes, where 15 minutes was assumed

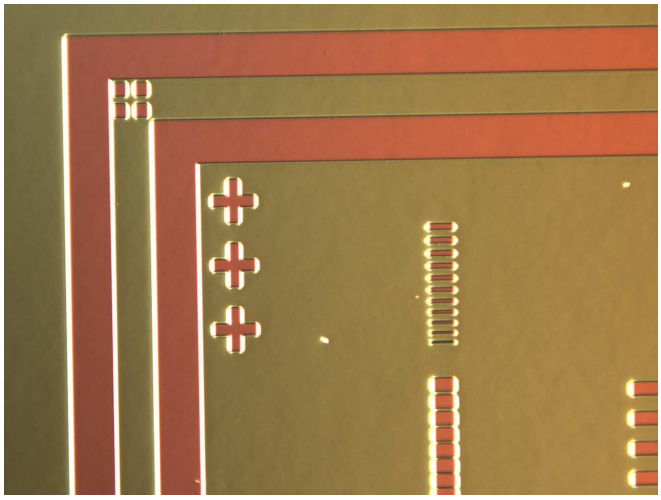

FIG. 2. Microscope shot of edge of sample after mask 1 has been exposed and developed.

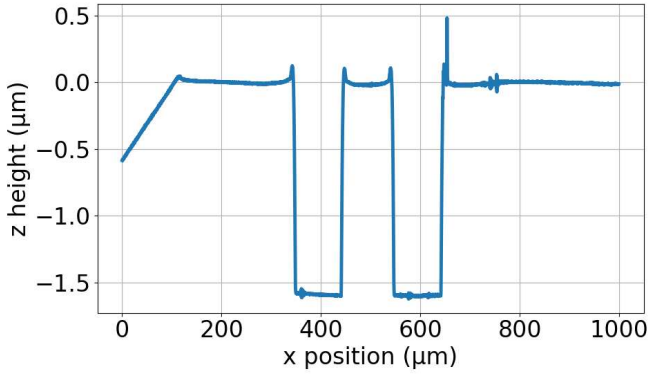

FIG. 3. Profilometer measurement of edge of sample after mask 1 BHF etch, before photoresist was removed. Note that this is the step directly before mask 1 oxidation.

to go to predeposition and 5 minutes to warming the samples.

During phosphorous predeposition, a layer of phosphor glass was grown on the surface of our samples. This is undesirable since the phosphor glass acts as a source of dopants, and should thus be removed. We etched off the phosphor glass layer by dipping our samples in BHF for the appropriate amount of time as determined by the water bead test on a pilot sample. If phosphor glass is present, a water bead will spread out. After removal, the water beads up, and the amount of time taken for this effect to be observed on the test sample was the amount of time that our samples were dipped in BHF.

Following phosphorous predeposition, we measured the sheet resistance and resistivity of the top surface of the test sample. Four-point probe measurements found a sheet resistance of $21.93\,\Omega/\square$ and resistivity was calculated by 1 to be $1.162\,\Omega\,\mathrm{cm}$. Carrier concentration was calculated according to 2 to be $2.25\times10^{17}\,\mathrm{cm}^{-3}$, confirming the presence of shallow, highly concentrated dopants.

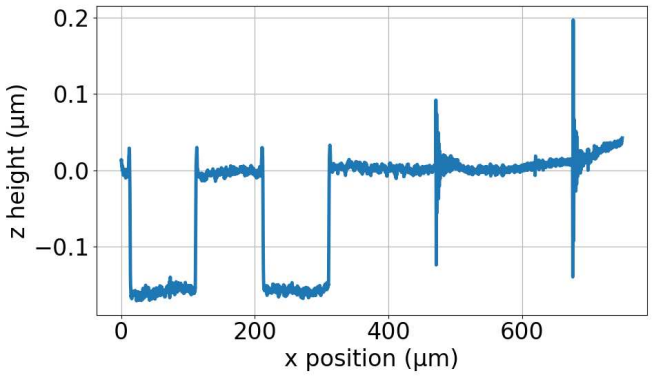

FIG. 4. Profilometer measurement of edge of sample after mask 1 oxidation.

C. Mask 2

The samples were recleaned according to the standard solvent cleaning procedure. After soft baking, we aligned three of our four samples to Mask 2(Fig. 5), keeping Sample 1 as a backup. Since this was the first alignment for Mask 2, we initially aligned, exposed, and developed Samples 3 and 4, then inspected them under a microscope to ensure proper alignment with the previous mask. After confirming the alignment was accurate, Sample 2 underwent the same process. This lithography step closely follows the procedure used for Mask 1, but with a much tighter alignment tolerance to the previous mask as mask 3 and 4 will also align on top in later step. Due to this precision requirement, We had to strip the PR with acetone and restart the photolithography process multiple times because the alignment with Mask 1 was not always precise.

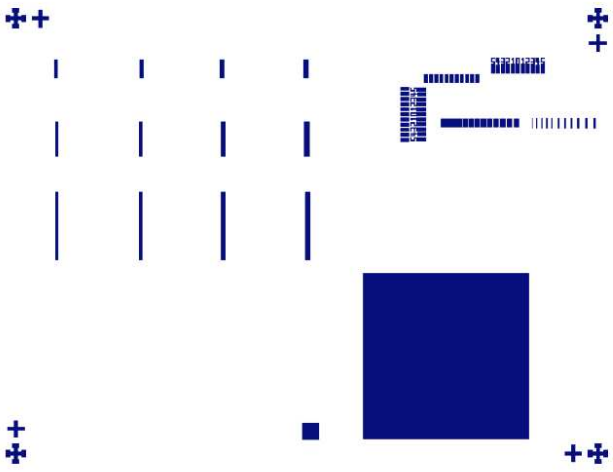

FIG. 5. Mask 2

After successful mask alignment, the sample underwent Plasma descum to be cleaned before undergoing HF

etch. We calculated the etch rate using a test sample and found the etch rate to be 1070.4 A/min. Given our oxide thickness as measured by the profilometer, the samples were etched for 5 minutes and 9 seconds including a 20% overetch.

Next, a dry oxidation process was performed to form 50 nm of high quality gate oxide. The time required to grow this oxide was calculated using the BYU oxide thickness calculator to be 38 minutes. The gate oxide thickness was confirmed with Filmetrics to be 45.8 nm.

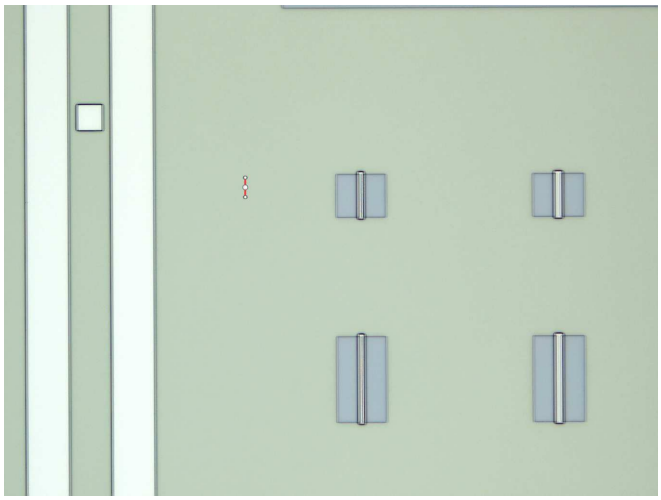

FIG. 6. Microscope shot of portion of MOSFET array after mask 2 BHF etch.

D. Mask 3

We repeated the lithography process described above, aligning Mask 3 (Fig. 7) to the samples.

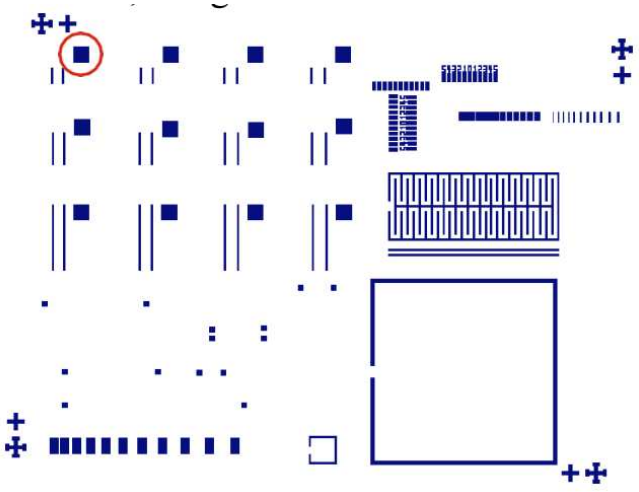

FIG. 7. Mask 3

After soft baking the samples after PR application, we realized that the samples contains contaminant and non-uniform thickness of PR, which is a result of dirty PR pipette. Cleaning the PR pipette and the PR container, and redoing the PR application got rid of the issues. After exposure, development, and hard baking, we inspected the samples under the microscope and took microscope images of the important regions where we realized that one of the capacitors of S2 contained contaminant and strange artifacts. We then proceeded to redo lithography for S2 and the artifact seemed to go away under microscope inspection. We then plasma descum the samples, and retake microscope images of the samples and characterized the side cut profile of the samples using the profiometer.

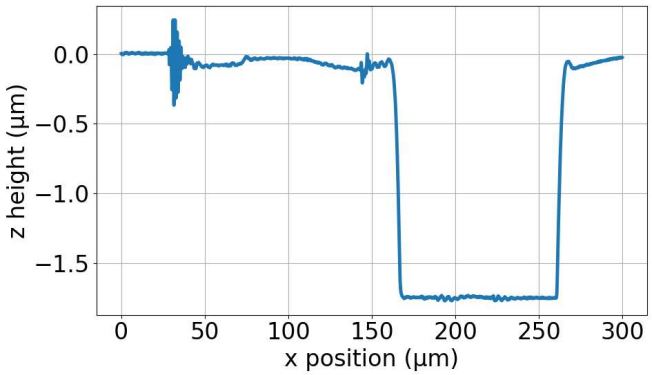

FIG. 8. Profilometer measurement of edge of sample after mask 3 BHF oxide etch.

E. Mask 4

Before patterning the final mask layer on the sample, each sample went through the standard acetone cleaning procedure outlined above. After the 3 minute hard bake at 120°C, HMDS vapor was deposited for 3 minutes. AZ P4110 photoresist was subsequently spun onto each sample for 30 seconds at 4000 RPM followed by a 1 minute soft bake at 94°C. Unfortunately during the photoresist application process, a fabrication wipe was improperly applied, hitting the sample during the spin, causing complete destruction of the sample. The aftermath is shown in Fig. 9.

Using the Karl Suss MJB3 Aligner once again, mask 4 (shown in Fig. 10) was aligned to mask 3 using the edges of the mask as well as the alignment marks near the corners. Then the sample was exposed for 18 seconds (previously calculated above). Afterward, the samples were dipped in toluene for 5 minutes and then blow dried with N2 gas. No water rinse is completed for this step. The samples were then developed in fresh AZ 400K for 100 seconds. The toluene was used to decrease the solubility of the top layer of the exposed photo resist. This creates a more pronounced overhang after development which helps with the lift off process along with the increased

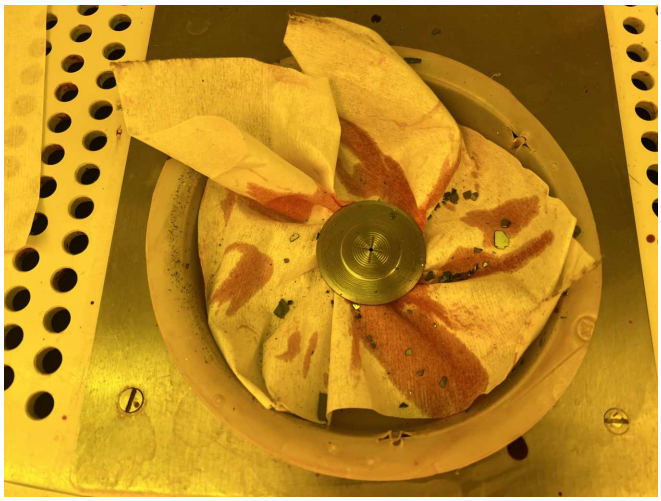

FIG. 9. During the application of the photoresist for mask 4, a fab-wipe was placed under the vacuum chuck to catch and stray photoresist. However, the fab-wipe accidentally got pinched by the vacuum chuck when it was inserted, which caused it to spin along with the vacuum chuck. This caught the edge of the sample and flung it off the side of the vacuum chuck, which blended the sample into many pieces. This image is included in the report as an example for what can happen if one is not careful in ensuring that the vacuum chuck is operating correctly. We have properly cleaned the vacuum chuck, ensuring that no residuals remain.

development time. Next, an oxygen plasma descum was conducted to remove any remaining photoresist.

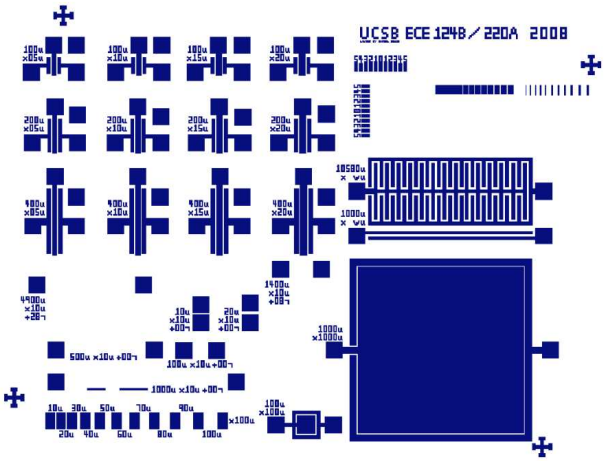

FIG. 10. mask 4 pattern

Microscope pictures(Fig. 11 & Fig. 12) and profilometer measurements(Fig. 13) were taken. Sample 3 had a misalignment of 0.05μm vertically and 0.05μm horizontally while Sample 4 had a misalignment of 0.05μm vertically and .1μm horizontally. The profilometer shots show a feature depth of 4.47 μm.

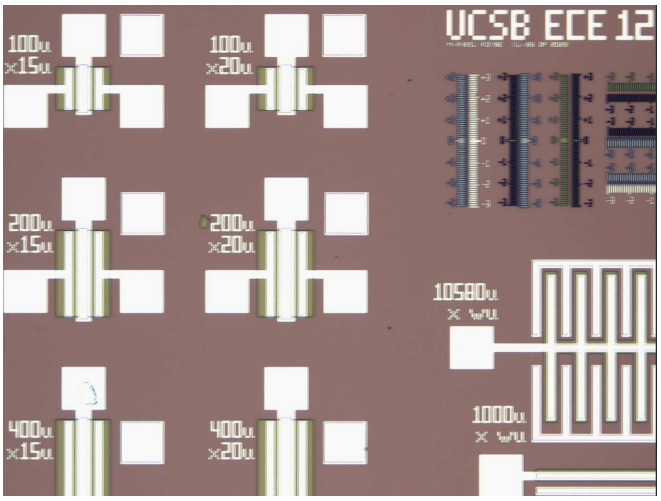

FIG. 11. Microscope shot of sample 3 after mask 4 O2 descum

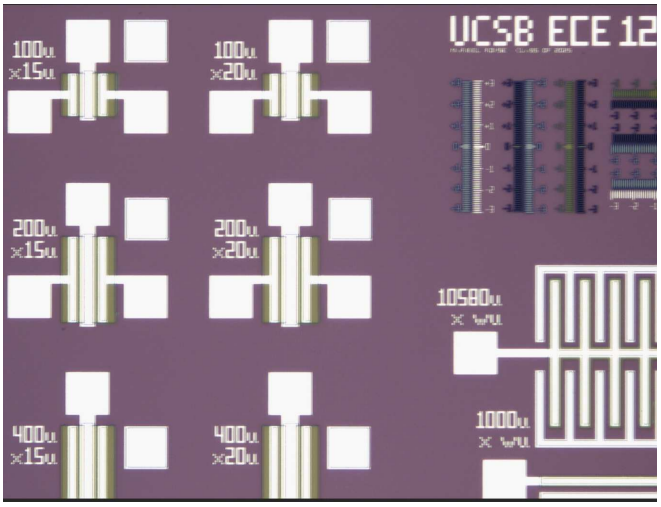

FIG. 12. Microscope shot of sample 4 after mask 4 O2 descum

F. Metal Evaporation & Liftoff

Prior to metallization, the samples were dipped into a buffer hydrofluoric acid for 10 seconds. This removed any native oxide that had grown on the samples. The samples were then handed over to the teaching assistants so that metal evaporation and liftoff could be performed overnight.

300 nm of aluminum was evaporated onto the sample using the Temescal TLAB^{tm} Electron Beam Evaporator. The evaporator melts aluminum at 660° C with 330mA of current. This is deposited onto the sample at a rate of 3 Å/s. Once the aluminum was successfully evaporated onto the sample, it was left overnight in a beaker of acetone. This removed all the remaining photoresist, which takes off any unwanted metal as well. Following successful liftoff, we solvent clean the samples and took microscope images (shown in Fig. 14) and profilometer data of the edges to ensure proper metal liftoff.

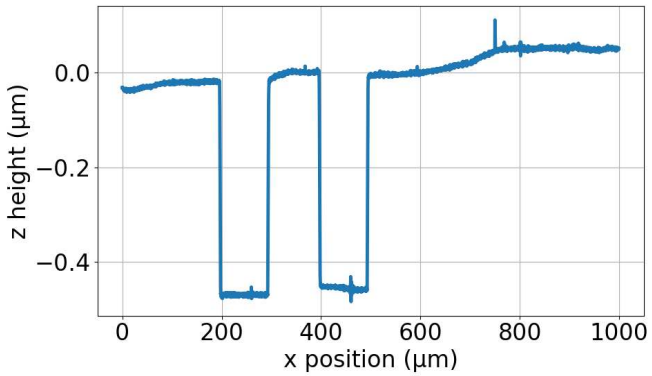

FIG. 13. Profilometer measurement of edge of sample after mask 4 BHF oxide etch.

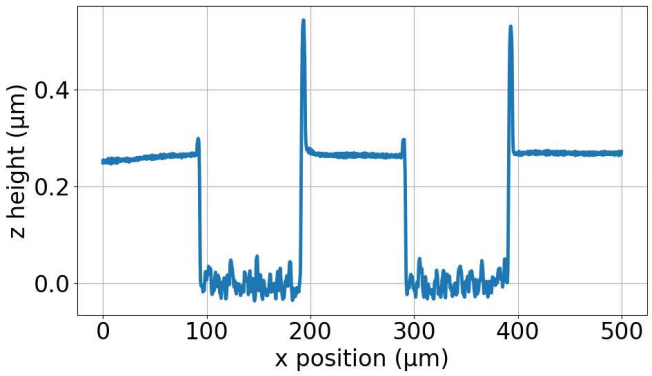

FIG. 15. Profilometer z-height measurement of edge of sample after metal liftoff.

G. Device Characterization

The device characterization included the MOSFETS, TLM pads, diodes, capacitor, and MOSCAP. We begun with MOSFETS characterization on S3 and S4 where we see the expected I-V curve on S3 16, but only noise on the order of *nm* for S4. We then proceeded to measure the TLM pads and the result indicates an Ohmic behavior 26, indicating that the device did not need further annealing. We also realized that the I-V curve contained discontinuity at positive V which was a result of poor electrical contact of the electrical test bench. After securing the cables and wiring of the electrical probes, the discontinuity in the measurements disappeared. We then proceeded to characterize the rest of the electrical components on our device.

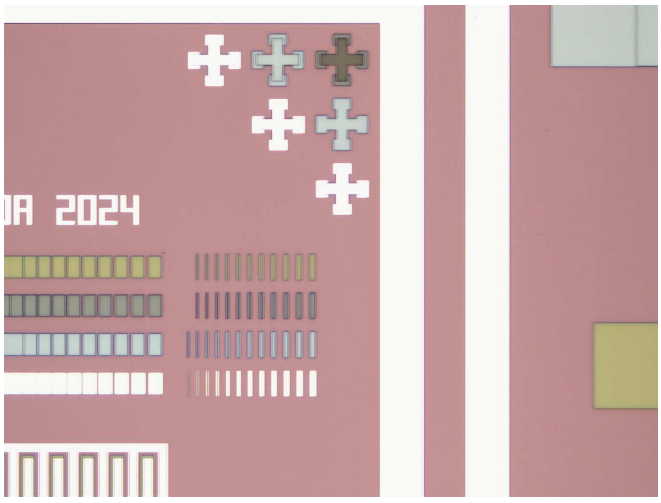

FIG. 14. Post metal lift off microscope shot. Note the drastic change of color compared to the previous microscope shots. Also note the alignment of the crosses inside each other, which indicates that mask 4 was aligned well to mask 3.

III. RESULTS & ANALYSIS

In this section, we will discuss the electrical characterization on sample 3.

A. MOSFET Measurements

All sizes of MOSFET had been characterized with I-V sweeps and I-V curves were generated for each MOSFET; an example of one of these curves is shown in Fig. 16.

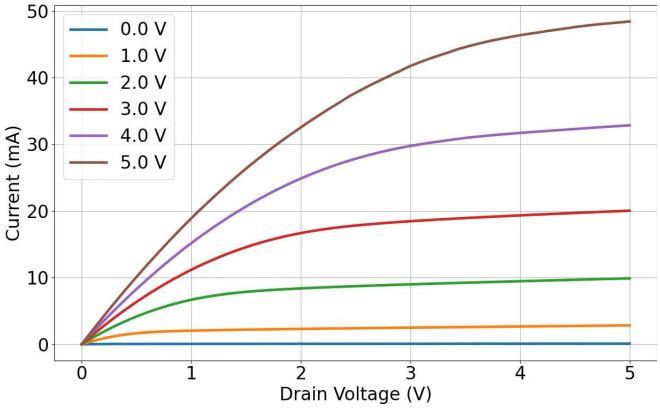

FIG. 16. I-V curves of a 400x5μm MOSFET for different stepped-through gate voltages.

Taking lengths and widths into account, we made a third-order polynomial fit for the data. This generates a 5-dimensional polynomial that describes the data with $R^2 = 0.9658$. This was done in order to generalize all of the data into one effective model—error is reduced dramatically since we have many more data points. We took 3D "cross sections" of this 5-dimensional phase space (separately at constant length and width) to depict how the general shape characteristic "fingerprint" of the MOSFET changed as a function of length and width. We found that as length increases, the current passing

through the MOSFET increases only for large gate voltages, whereas the opposite is true for width—that is, as width increases, current at large gate and drain voltages decreases. This is also a very significant effect; the maximum current changes nearly tenfold. Videos of the 3D plots are included in this paper's appendix.

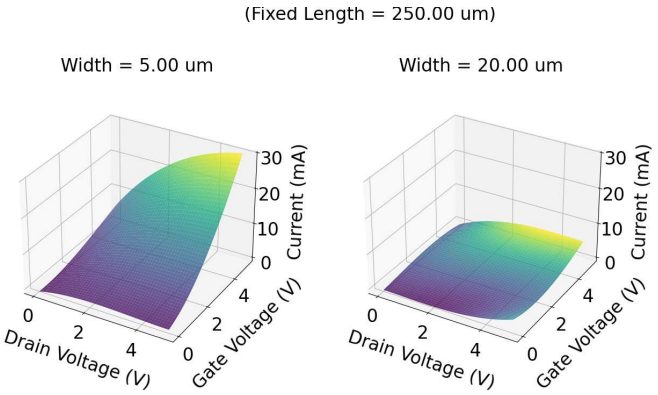

FIG. 17. 3D slice of 5D MOSFET phase space for both small and large MOSFET widths (at fixed length). Here, we can see that the gate voltages decrease as MOSFET width increases.

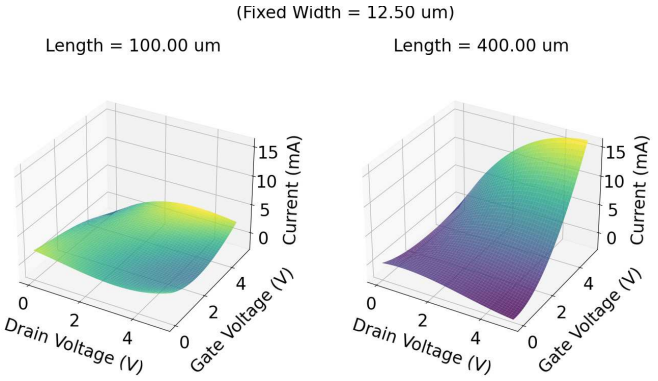

FIG. 18. 3D slice of 5D MOSFET phase space for both small and large MOSFET lengths (at fixed width). Here, we can see that the gate voltages increase as MOSFET length increases.

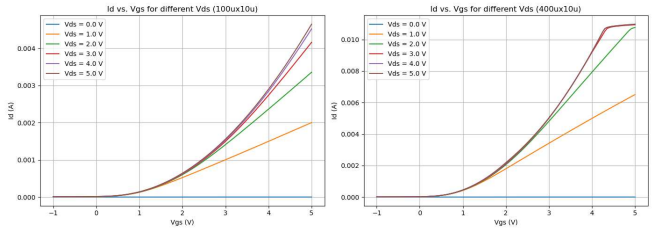

FIG. 19. I_d-V_{gs} curve of 100 µm x 10 µm (left) and 400 µm x 10 µm (right) MOSFET for different stepped-through drain voltages.

Next, we measured the drain-source current (I_{ds}) vs. gate-source voltage (V_{gs}) with stepped drain-source voltages (V_{ds}), for gates of varying sizes. Specifically, we picked 100 µm x 10 µm and 400 µm x 10 µm, as shown in Fig. 19. As V_{gs} increases above a certain point (roughly 0.7-1 V), the drain current I_{ds} begins to rise significantly. This is the expected turn-on behavior for an NMOS, and 0.7-1 V is the threshold voltage V_t. 400 µm x 10 µm MOSFET shows an overall current higher than the 100 µm x 10 µm one. This is expected because increasing the channel width (W) increases the drive current of the transistor (roughly proportional to W/L for the same bias conditions). Also, this allows the transistor with larger channel width to reach pinch-off at a lower drain-source voltage. As a result, the 400 µm device saturates at a lower voltage than the 100 µm device. The transconductance (g_m) for each MOSFET can be calculate by the equation below:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{4}$$

where I_d is the saturation drain current. Through calculation, the 100 µm x 10 µm MOSFET has a transconductance of 1.923mS and 400 µm x 10 µm one is 5.14mS. This is expected as g_m is directly proportional to $\frac{W}{L}$.

We have also measure the breakdown voltage of three MOSFETs: 100 µm x 10 µm, 200 µm x 5 µm, and 200 µm x 10 µm. As shown in Fig. 20, all of the MOSFETs have similar breakdown voltages at ∼18 V, and the discrepancy between how steeply they rise is related to the intrinsic resistance of that part of the sample—that is to say, the longer gate width and length will have a higher resistance, so the current will initially rise more steeply. Included in Fig. 21 is an image demonstrating the exact capacitor that was broken down in our measurements.

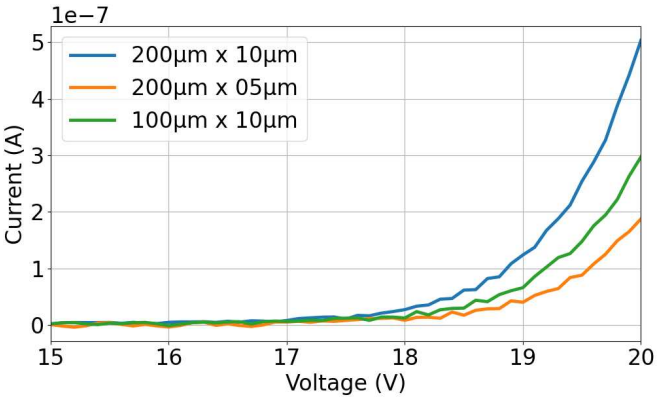

FIG. 20. Three separate MOSFET I_{ds}-V_gs curves for the breakdown experiment, probing across the gate and body-bias contacts.

CV measurements were also taken for the moscaps. These are shown in Fig. 22 and 24. We found that for smaller gate sizes(Fig. 25, the capacitance was proportionally smaller as well, while keeping similar shapes to Fig. 22. This makes sense as the capacitance is essentially a parallel plate capacitor, which is proportional to

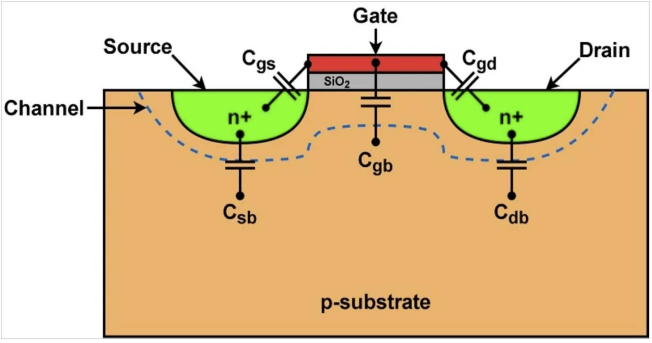

FIG. 21. Parasitic capacitance model of the MOSFET showing physical intuition of our measured capacitance (C_{gb}) [2]

the area. The flatband voltage can be extracted from the CV graphs by finding the voltage at which the capacitance becomes constant. For our moscaps, the flatband voltage was 5.7V. Although CV measurements are sensitive to electrical traps and charges at the interface, we felt that our CV curves were accurate and were not significantly detrimented by our sample preparation, see comparison between Fig. 22 and Fig. 23. We did not see a difference in performing the results under darker conditions.

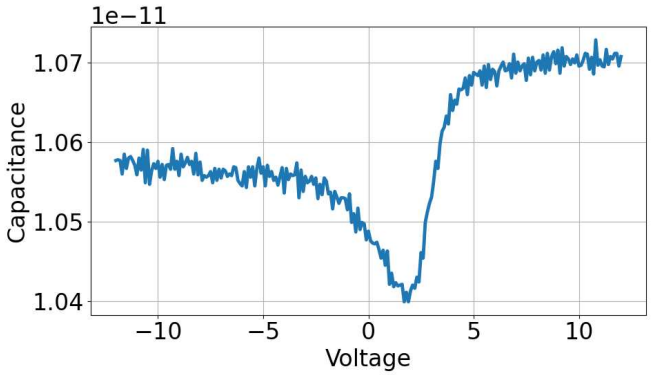

FIG. 22. C-V curve of the MOSCAP, probing across the gate and the body-bias. This should act like an effective resistor, which is why the same measurement was conducted for a pure resistor, depicted in Fig. 23. Note that the two figures have extremely similar shapes, with similar orders of magnitude. Thus, we are confident that this MOSCAP measurement does indeed reflect the behavior of a resistor.

B. TLM Measurements

I-V curves were taken for each of the TLM pad separation distances. The center ohmic region of each I-V curve was used to compute a least-squares regression line, an example of which is depicted in Fig. 26. These slopes correspond to the inverse of the resistance between both of the probes. Note that every single fit was extremely

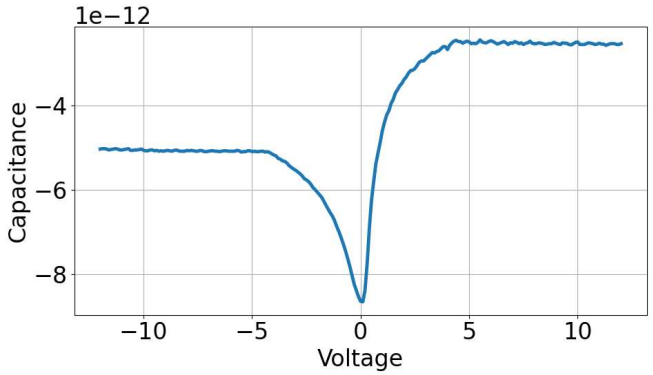

FIG. 23. C-V curve of a 500 µm x 10 µm resistor. This measurement was conducted as a control for the measurement in Fig. 22.

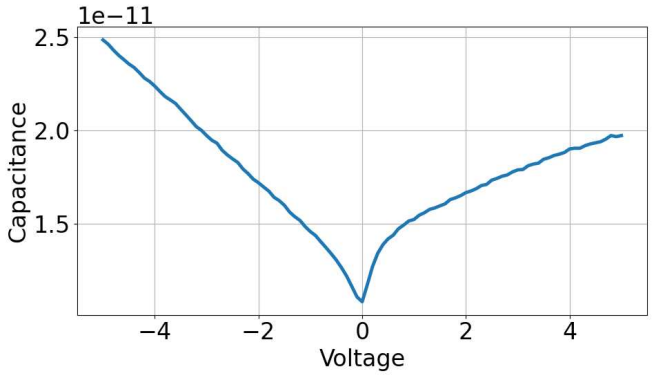

FIG. 24. MOSCAP C-V curve. Here, we are probing a 200 µm x 10 µm MOSCAP across the source and the drain.

good, with an R^2 value of at least 0.99. This differs from the results of our previous paper, which required annealing for the TLM I-V curves to demonstrate strictly ohmic behavior; an example of the same TLM pad separation of 80 µm from our Lab 4 paper is depicted in Fig. 27. Thus, we did not need to anneal our samples for the following measurements.

The resistances computed from the reciprocal of the LSRL slopes were all plotted on the same graph, and the LSRL was computed. This LSRL represents the change in the resistance between the two probes as TLM pad separation changes. The slope and y-intercept of this line was used to calculate the contact and sheet resistances of the sample, whose relationship are demonstrated in Eq. (5).

$$R_{\text{total}} = 2R_{\text{contact}} + \left(\frac{R_{\text{sheet}}}{W}\right) L \tag{5}$$

Interestingly, both the sheet and contact resistances were on the order of several ohms—around 6.0 and 4.5 Ohms, respectively. It's generally difficult to have an intuition for whether this is a large resistance since both the cross-sectional area and the length are extremely small.

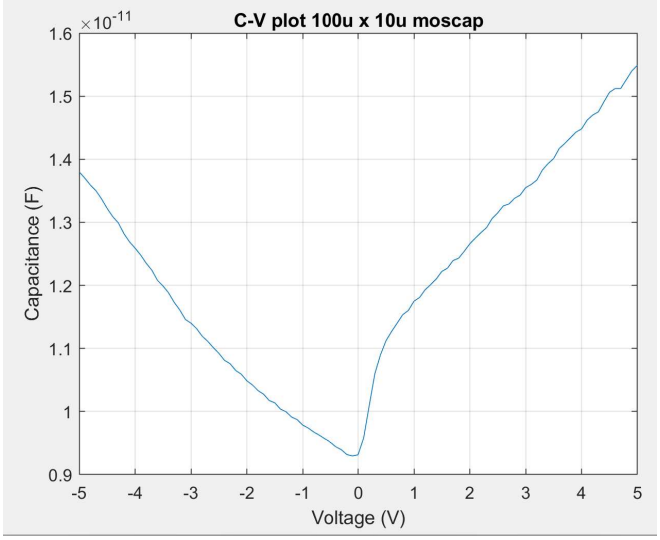

FIG. 25. MOSCAP C-V curve. Here, we are probing a 100 µm x 10 µm MOSCAP across the source and the drain. Notice the lower magnitude of capacitance compared to the larger gate 24

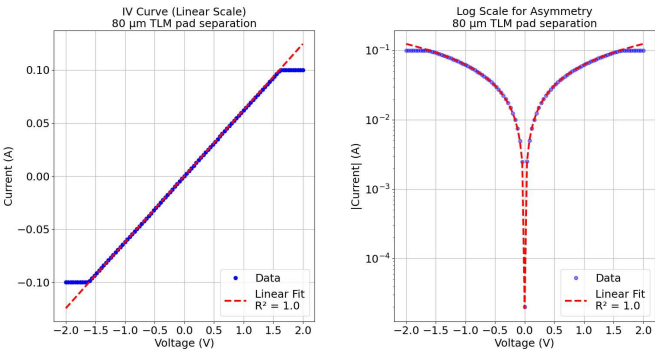

FIG. 26. Selected transmission line measurement. This is a TLM pad I-V curve measurement for two TLM pads with 80 µm separation. A linear fit has been done on the middle region for all serparations. This figure serves as an example of what all TLM I-V curves look like. The slopes of the LSRL lines from each TLM I-V curves are plotted in Fig. 28, where contact and sheet resistance are calculated.

However, this is slightly higher than the same resistances from our samples in Lab 4, which were each around 2 Ohms. This is most certainly because those samples were annealed, since their pre-annealed resistances were on the order of kilo-Ohms.

An IV measurement of the resistors were taken as well to ensure proper device functionality. The $10\mu m$ x $10\mu m$ plot is shown in Fig. 29. It displays ohmic behavior from 1V to 5V.

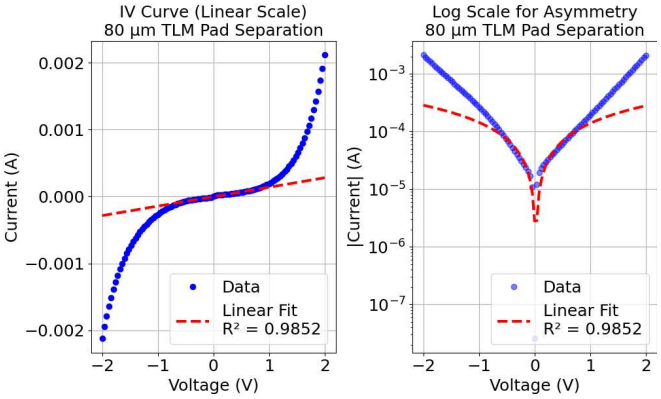

FIG. 27. Lab 4 pre-annealed I-V curve of TLM with 80 µm pad separation. Note the stark difference with this result and the same result in this paper (depicted in Fig. 26), which was also not annealed. The Lab 4 TLM I-V curves only demonstrated a sensible ohmic region after annealment. The process of annealing consistes of heating and applying Hydrogen gas to pacify the surface charge of the silicon caused by dangling bonds. What may have happened was that during the DI water rinse after HF etch, loose hydrogen particles could have pacified the surface which we deposited metal directly onto. Thus creating a Ohmic contact without undergoing Annealing

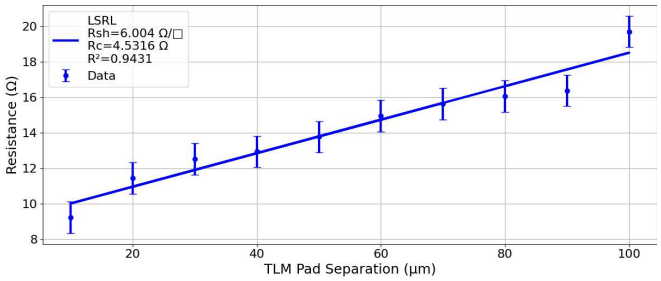

FIG. 28. Resistances from all TLM pad measurements. The slope and y-intercept of the LSRL of this data are related to the sheet and contact resistances. These were computed from Eq. (5). Error bars were computed using the standard deviation of the measurements.

C. Diode Measurements

Electrical measurements were taken on the 1000 μm diode using the two point probe. First, a voltage sweep of -2V to 2V was applied across the diode and the current was measured. The IV curve of the 1000 μm diode (Fig. 30) demonstrates a threshold voltage of around 0.2V. The 10580 μm diode displays similar behavior(Fig. 31 The curve does not demonstrate the ideal exponential diode curve as outlined in Eq. 6. Instead, the current has a sublinear shape, which might be caused by poor probe-diode contact.

The dark current of the diode, or the reverse leakage current at -2V was found to be $-4.24\mu A$ for the $1000\mu m$ diode and $-5.58\mu A$ for the $10580\mu m$ diode. The ideality factor or n can be calculated from Eq. 6 The ideality

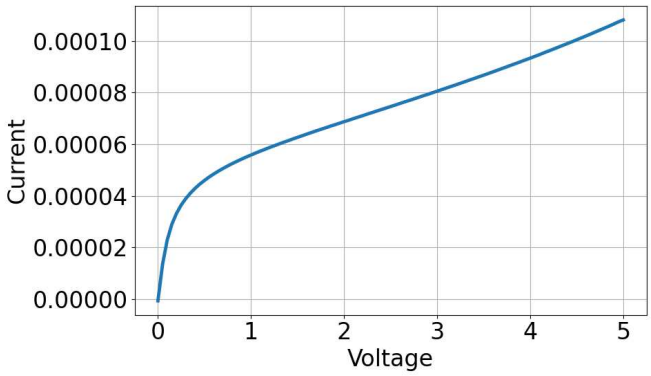

FIG. 29. I-V curve of a 10u x 10u resistor. Note the Ohmic region is between 1 and 5 V.

factor of the 1000 μm diode was found to be 1.912 and the ideality factor of the 10580 μm diode was found to be 1.914. The series resistance of each diode was calculated using Ohm's law in the linear region. This yielded a series resistance of 0.0014Ω for the 10580 μm diode and a series resistance of $1.5 * 10^{-4}\Omega$ for the $1000\mu m$ diode. [3] This resistance is oddly low because of the sublinear nature of our IV curves. This sublinear behavior could be explained by lack of proper contact now allowing the full current to flow.

$$I = I_s \left(e^{\frac{V}{nV_T}} - 1 \right) \tag{6}$$

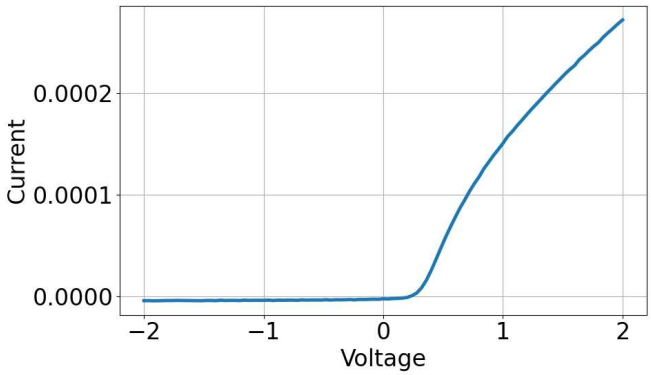

FIG. 30. I-V curve of a 1000 µm long diode before a breakdown voltage was applied.

To measure the breakdown voltage of the diodes, negative voltage was applied increasingly, until the maximum negative limit of the machine was reached. The 1000 μm results are shown in Fig. 32. Similar results were found for the 10580 μm diode. The IV curve shows no change in current–mostly noise all the way until the maximum negative voltage. This means that the breakdown voltage for both diodes is greater than -40V.

Finally, C-V measurements were taken on both diodes (Fig. 33 & 34). The built in voltage is found using

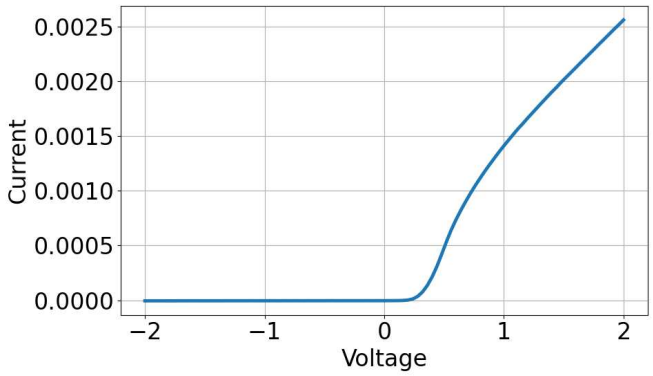

FIG. 31. I-V curve of a 10 580 µm long diode before a breakdown voltage was applied.

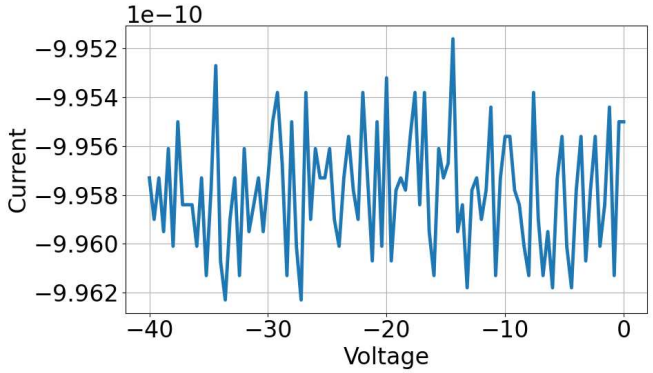

FIG. 32. I-V curve of a 1000 µm long diode. Here, we were attempting to apply a breakdown voltage but couldn't with the instrumentation we were using (note the scale on the y-axis; the fluctuations here are likely due to noise). Other groups found their diode breakdown voltage to be near −70 V, which is in a regime not accessible to us at the time of measurement.

the relationship outlined in Eq. 7 [2]. The equation shows that by finding the x-intercept of graph, we should be able to determine V_{bi}. Unfortunately, our measurements do not include data where the capacitance reaches 0. Thus, a typical built-in voltage value of 0.9V will be used in future calculations. [4]

$$\frac{1}{C^2} = \frac{2(V_{bi} - V)}{q\epsilon_s N_A} \tag{7}$$

To find the acceptor concentration, Eq. 7 is used. Using $\epsilon_s = 11.7 * 8.85 * 10^{-14} F/cm$ and substituting the slope of the graph into the equation, we get an acceptor concentration of $2.19 * 10^{14} cm^{-}3$ for the $10580\mu m$ diode and $1.69 * 10^{1}3cm^{-}3$ for the $1000\mu m$ diode.

It can be seen in 35, the capacitance of the IV measurement is measured to be negative, this is due to the current lagging behind the voltage instead of aligning with the expected 90° lead of current in ideal capacitors. During the voltage sweep, the measured impedance response may have been influenced by parasitic resistance and in-

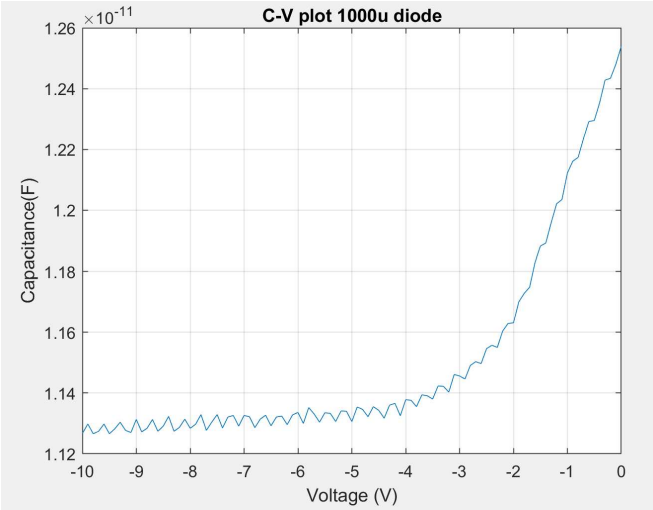

FIG. 33. C-V curve of the 1000 µm diode.

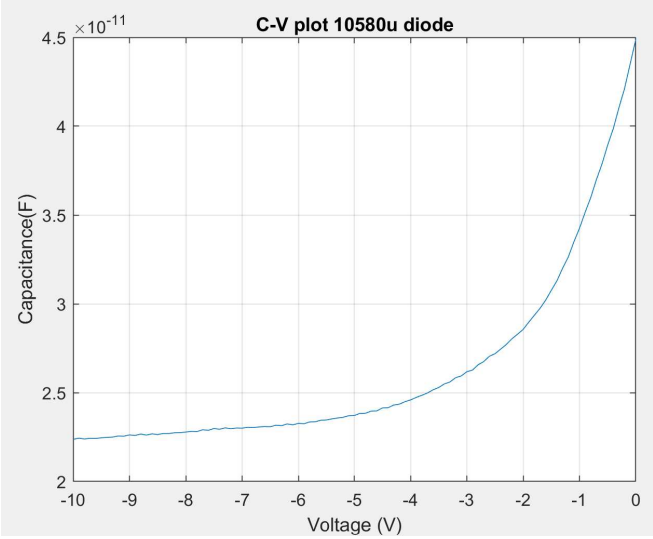

FIG. 34. C-V curve of the 10 580 µm diode.

ductance in the circuit, causing it to be negative.

IV. CONCLUSION

The fabrication and characterization of MOSFETs, diodes, MOSCAPs, and resistors provided critical insights into semiconductor device physics and processing. Key achievements include the successful fabrication of functional n-channel MOSFETs with a gate-to-body breakdown voltage of 18 V, TLM structures demonstrating ohmic behavior without requiring post-fabrication annealing, and diodes exhibiting breakdown voltages beyond the measurable limit of −40 V. The electrical characterization validated the importance of precise process control, particularly in photolithography alignment and etching steps, which directly impacted device performance.

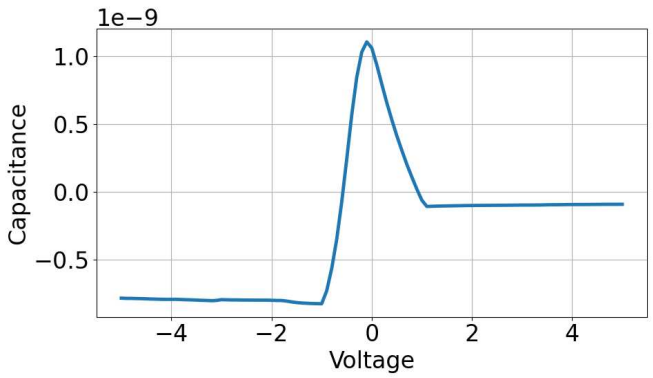

FIG. 35. C-V curve of the very large 1000 µm x 1000 µm parallel plate capacitor. This serves primarily as a "sanity check" for the rest of our C-V curves, particularly for the transistors, as this gives a good reference for what a typical capacitor C-V curve should look like.

Challenges such as photoresist contamination, mask misalignment, and accidental sample destruction during fabrication underscored the sensitivity of semiconductor processing. These issues were mitigated through iterative process refinement, including improved alignment techniques and rigorous cleaning protocols. The results from the surviving samples confirmed the viability of the fabrication sequence, with MOSFET I-V curves and TLM resistance measurements aligning closely with theoretical expectations.

The C-V analysis of MOSCAPs and resistors further reinforced the relationship between geometric design and electrical behavior, while diode characterization highlighted the robustness of the PN junction under high reverse bias. Future work could focus on enhancing alignment precision for multi-mask processes and exploring annealing effects on contact resistance. Overall, this lab demonstrated the intricate balance between theoretical principles and practical execution in semiconductor device fabrication, providing a foundational understanding essential for advanced integrated circuit design.

V. AUTHOR CONTRIBUTIONS AND ACKNOWLEDGMENT

We would like to show our greatest appreciation to the lab manager, Dr. Prashant Srinivasan, and the TAs. It would be impossible for us to successfully build the device without constant support and helpful instructions during every lab section. The following is the table of author contributions.

Section	Contributor(s)
Abstract	Maxwell
Introduction	Maxwell
	Thomas
Methodology	Deven
	Maxwell
	Chengxuan
	Robin
Results & Analysis	Maxwell
	Mark
	Thomas
	Robin
	Chengxuan
Conclusion	Thomas

VI. APPENDIX

This appendix provides access to all the relevant files and Python code used in the experiment. These resources provide all the details necessary to replicate the experiment, analyze the data, and generate the plots presented in the paper. The link below leads to all resources:

- `https://github.com/markzakharyan/ECE-120A`

[1] solecon, How do we calculate carrier concentration?, (2025), accessed: March 17, 2025.

[2] N. S. John, Mosfet non-idealities in analog ic design, All About Circuits (2023).

[3] P. Education, Diode equation, PVCDROM - PN Junctions (2025), accessed: March 17, 2025.

[4] C. Hu, Chapter 4.1: Mosfet theory and design, UC Berkeley (2020).